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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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10679 U.S. PTO
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INVENTOR(S)					
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Charles Eugene Miron		Stroud Abramovici		Charlotte, North Carolina Berkely Heights New Jersey	
<input type="checkbox"/> Additional inventors are being named on the _____ separately numbered sheets attached hereto					
TITLE OF THE INVENTION (500 characters max)					
BIST - Based Delay-Fault Testing in FPGAs					
Direct all correspondence to: CORRESPONDENCE ADDRESS					
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<input checked="" type="checkbox"/> Firm or Individual Name		University of North Carolina at Charlotte			
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ENCLOSED APPLICATION PARTS (check all that apply)					
<input checked="" type="checkbox"/> Specification		Number of Pages 9		<input type="checkbox"/> CD(s), Number	
<input checked="" type="checkbox"/> Drawing(s)		Number of Sheets 4		<input type="checkbox"/> Other (specify)	
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METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT					
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Respectfully submitted,

SIGNATURE

Charles E. Stroud

Date

07/28/2002

TYPED or PRINTED NAME Charles E. Stroud

TELEPHONE 704-687-4144

REGISTRATION NO.
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UNCC#2002-034

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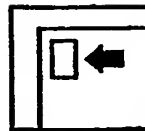
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REPORT OF INVENTION

1. Report Date: June 25, 2002

2. **Inventorship:** (Identify all inventors below. In Section 2 (a), if all inventors are UNCC students, staff and/or faculty, place a checkmark next to the first item. If inventors include students, staff, and/or faculty external to UNCC, place a checkmark next to the second item. In Section 2 (b), list contact information for all inventors, identifying the primary contact person in Section 2 (b)(i))

a. UNCC Only _____ UNCC + External X
b. Inventors:

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3. **Sponsorship:** (Identify any and all sponsors below who have contributed cash and/or in-kind funding/assistance for the efforts associated with this invention. If none, write "n/a" in all spaces provided.)

a. Sponsor Name(s): DARPA via subcontract through Agere Systems
b. UNCC Contract/Grant No.: 555422
c. Funding Period: July 1, 2000 – December 31, 2001
d. Principal Investigator (PI): John M. Emmert

4. Title of Invention: BIST-Based Delay Fault Testing in FPGAs

PATENT PRIMER

According to the United States Patent and Trademark Office ("USPTO"), patents may be issued for inventions that are novel, nonobvious, adequately described to allow one of ordinary skill in the art to make and use the invention, and claimed by the inventor in clear and definite terms. Patentable inventions include: process, machine, article of manufacture, composition of matter, and improvement of the preceding items. Such patents are defined as "Utility Patents". Patent protection is also available for: (a) ornamental design of an article of manufacturer ("Design Patents"), (b) asexually reproduced plant varieties ("Plant Patents"), and (c) business processes and models ("Business Patents"). Items that cannot be patented: laws of nature, physical phenomena, abstract ideas, literary/dramatic/musical/artistic works (which can be copyright protected.)

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Pursuant to Policy Statement #7, "Patent and Copyright Procedures" of the University of North Carolina at Charlotte ("UNCC"), The University of North Carolina Patent and Copyright Policies, and all other UNCC employment and intellectual property policies and procedures, I/we hereby disclose details about the following invention:

5. **Invention Abstract:** *(Attach a one paragraph summary description of your invention. Identify whether invention is a new process, composition of matter, a device, software, one or more products, a new use for or an improvement to an existing product or process.)*
We have developed a process by which Field Programmable Gate Arrays (FPGAs) can be tested for delay faults using Built-In Self-Test (BIST) techniques. The FPGA is programmed with BIST circuitry which specifically tests the programmable logic and interconnect resources within the FPGA for delay faults. Once the device has been tested, the FPGA can be re-programmed with the intended system function. This allows delay fault testing using inexpensive test equipment during manufacturing testing as well as either on-line or off-line system level testing. See attachments for more details.
6. **Field of the Invention:** *(Describe to what field the invention relates.)*
7. **Description of Related Art:** *(Describe all known related, prior art, including published literature, commercial products, and related patents and other forms of intellectual property, and conclude with a summary listing of all known related art.)*
8. **Detailed Description of the Invention:** *(Describe in detail the nature, operation, preferred embodiment, and applications of the invention. What technical problem does this invention solve, and for whom is this a problem? Include details of how this invention is nonobvious to those skilled in the art, novel, and useful – how does it differ from the prior art?)*
9. **Figures and Drawings:** *(Attach all related figures and drawings that help to describe the nature, operation, and applications of the invention.)*
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12. **Regulatory Requirements:** *(Does this technology require approval by regulatory agencies EPA, USDA, FDA, OSHA, other? If yes, please explain.)*
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 - a. **Potential Markets:** *(Briefly identify a few potential markets for this invention and how this invention addresses each market's specific needs.)*

- b. **Competition:** *(Identify all known competing approaches to solving the problems addressed by this invention, as well as all commercial competitors and prospective competitors.)*
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15. **Inventor Signatures:** *(By signing below, I acknowledge that I am one of the inventors of the invention reported herein. I understand that the University of North Carolina at Charlotte owns the rights to, and may obtain protection for, all intellectual property developed by its students, staff and faculty subject to the provisions of University policies and procedures. By signing below, I hereby agree to execute a formal assignment of all rights to the invention to the University, unless so noted below in Section 19 "Request for Waiver".)*

(i) Sign: _____ Date: _____
Print: Charles Eugene Stroud

(ii) Sign: _____ Date: _____
Print: Miron Abramovici

16. **Signature of Person Witnessing This Disclosure:** *(Obtain the signature of a colleague knowledgeable in the subject matter of this invention, who has read and understands the concepts presented herein, and who may be called upon to support the claims herein throughout the patent process.)*

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17. **Department Chairperson:** *(Obtain the signature of your department's Chairperson to acknowledge his/her understanding of this disclosure and the interrelationship between this invention, any related sponsored research, potential conflicts of interest, and University duties.)*

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18. **Office of Technology Transfer Signature and Date Recorded:**

Sign: _____ Date: _____
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19. **Inventor Request for Waiver:** *(Optional: If you believe that the invention was made outside the general scope of your University duties, conceived without the use of University time, facilities, staff, materials, University information not available to the general public, and without the use of funds administered by the University, check the space below, sign and date where shown (in addition to signing above), and provide a short explanation of the circumstances under which the invention was made and developed, resources employed, and your University duties at the time of the making of the invention. If you would like the University to consider patent prosecution of this invention in its name, check the appropriate space below as well.)*

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BIST-Based Delay-Fault Testing in FPGAs

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Abstract: We present the first delay-fault testing approach for FPGAs, applicable both for manufacturing and for on-line testing. Our approach is based on BIST, is comprehensive, and does not require expensive ATE. We have successfully implemented this BIST approach on the ORCA 2C series FPGA.

1. Introduction

Advances in VLSI technology have resulted in more defects affecting the delays in the circuit, thus increasing the importance of delay-fault testing. The current FPGA manufacturing testing practice relies on configuring the FPGA with many designs and running them at speed. This is useful for speed-binning, but it is not a comprehensive delay-fault test. One of the main difficulties of the problem of delay-fault testing for FPGAs originates in the fact that users' circuits are not known when the chip is manufactured. While for an ASIC the target clock frequency is known before the chip is fabricated, it is impossible for the FPGA manufacturer to test the circuits that will be implemented on each device. Previous work in FPGA delay-fault testing [7][8] considered only the testing of the user's circuit. However, such an approach is not acceptable either to the FPGA manufacturers, who want to ship defect-free chips, or to users, who want to purchase defect-free parts; otherwise, system-level debugging becomes a nightmare if design problems are intermixed with manufacturing faults.

In testing FPGAs, we can take advantage of their unique properties - reconfigurability, partial reconfigurability, and regular structure - to achieve features that cannot be realized in ASIC testing. Unlike in ASICs, where BIST requires large area overhead and some performance degradation, FPGA BIST can be done with zero area overhead and no delay penalty [10]. While exhaustive testing is practically impossible for ASICs, in FPGAs we can exhaustively test both the *programmable logic blocks* (PLBs) and the programmable interconnect network, both for off-line [4][12] and on-line testing [3][11] with reasonable test application times. Exhaustive testing guarantees maximum fault coverage and removes the need to evaluate the test quality. Thus FPGA test does not require either ATPG or fault simulation, which are computationally expensive tasks for ASICs. Accurate fault diagnosis is difficult to achieve in ASICs, but it can be done very efficiently in FPGAs [4][3][11]. In ASICs, fault tolerance for manufacturing faults cannot be accomplished without massive redundancy, but FPGAs allow efficient fault-tolerance without dedicated spare resources [5][6].

Our first attempt to do FPGA delay-fault testing was to run our BIST configurations at the specified clock rate for the target FPGA. However, we quickly realized that this cannot

work, unless we significantly increased the number of configurations. The number of configurations is the dominant factor determining the total test time, because the configuration time is several orders of magnitude larger than the pattern-application time. To limit the number of configurations, our BIST techniques try to test as many resources as possible within the same configuration. For off-line PLB test, this requires distributing the patterns from the test-pattern generator (TPG) to many PLBs under test using long signal paths. Similarly, for interconnect test, the wires under test are long, connecting many wire segments and switches. Under these conditions, we must run the BIST configurations at a frequency much lower than that used in normal operation, so most delay faults will not be detected by these tests. An alternative would be to reduce the amount of logic and/or interconnect that is under test during any BIST configuration to allow BIST execution at a higher clock frequency; however, this will require more configurations, and ultimately significant increases in testing time and cost.

In this paper, we introduce a novel technique for delay-fault testing in FPGA. Our technique is independent of the applications implemented on the FPGA, and it is applicable for both off-line manufacturing testing and for on-line testing (the latter in the context of the Roving STARs approach [3]). Our method is based on BIST, it is comprehensive, and it can work with any low-cost ATE. For our implementation, we used the Lattice ORCA 2C series FPGA [16], but our technique can also be applied to most other FPGA architectures, such as such as the Xilinx Virtex [17].

The remainder of this paper is organized as follows. In Section 2 we present the principle of the BIST technique, and in Section 3 we analyze its implementation issues. In Section 4 we discuss the application of the delay-fault BIST approach to on-line and off-line testing. Finally, we present conclusions in Section 5.

2. The Main Idea

An FPGA is composed of PLBs, programmable I/O cells, and programmable interconnect; the latter consists of wire segments that can be connected via programmable switches referred to as *configurable interconnect points* (CIPs). Wire segments in the programmable interconnect network are bounded by these CIPs and are considered to be either global or local routing resources. Global routing resources connect non-adjacent PLBs, while local routing resources connect a PLB to global routing resources or to adjacent PLBs. The routing resources are bus-oriented, with the number of wires per bus typically ranging between 4 and 8. The PLB functions and the CIPs are controlled by writing the configuration RAM.

The basic CIP structure consists of a transmission gate controlled by a configuration memory bit (Figure 1a). There are three types of CIPs which we refer to as the *cross-point CIP* (Figure 1b), the *break-point CIP* (Figure 1c), and the *multiplexer (MUX) CIP* (Figure 1d) [16]. While a cross-point CIP connects wire segments located in disjoint planes (a horizontal segment with a vertical one), a break-point CIP connects two wire segments in the same plane. The MUX CIP comes in two varieties: decoded and non-decoded. A decoded MUX CIP is a group of 2^k cross-point CIPs sharing a common output wire and controlled by k configuration bits, such that the input wire being addressed by the configuration bits is connected to the output wire; the decoding logic is incorporated between the configuration bits and the transmission gates. A non-decoded MUX CIP contains a configuration bit for each transmission gate, such that k wire segments are controlled by k configuration bits; usually only one of the configuration bits is active for any configuration. There is also a *compound CIP* (Figure 1e), which is a combination of four cross-point and two break-point CIPs, each separately controlled by a configuration bit [17]. Most recent FPGA interconnect architectures are primarily constructed from non-decoded MUX CIPs that are buffered to prevent signal degradation due to the series resistance of each transmission gate the signal passes through.

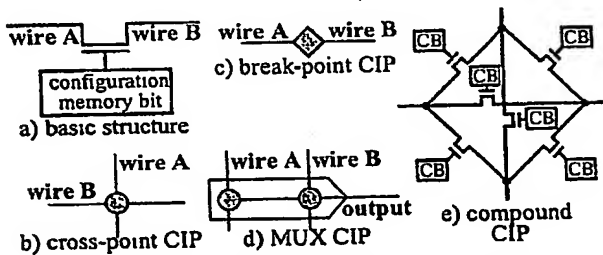


Figure 1. Configurable Interconnect Points

A signal path is formed by connecting several wire segments and PLBs in a continuous sequence via multiple CIPs. The propagation delay along the path accumulates the delays of all its PLBs, segments, and CIPs. A path may have different delays for rising (0/1) and falling (1/0) transitions.

Figure 2a illustrates our BIST architecture. We configure several *paths under test* (PUTs), so that every path has the same sequence of PLBs, wire segments, and CIPs. Each PLB on the path is programmed as an identity function, so it appears as a buffer for the signal propagating along the path. The PUTs are identical, except for their position in the FPGA. This works well with the bus structure of the programmable interconnect of most FPGAs (with 4 to 8 wires per bus).

Our technique compares the delays of the PUTs. Assume that a rising transition is applied at their common input I . This transition propagates along every PUT, and it will eventually appear at the inputs of the OR and the NAND gates. The signal *FIRST* responds to the fastest arriving transition, while *LAST* changes only after the slowest one has arrived. *FIRST*

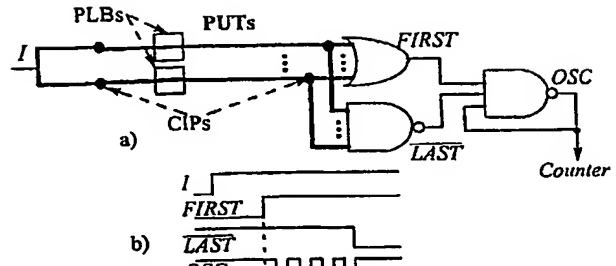


Figure 2. The basic principle

enables the local oscillator loop, and *LAST* stops the oscillations (see Figure 2b). Thus the count of *OSC* pulses measures the difference D between the fastest and the slowest propagation delays along the PUTs. In a circuit free of delay faults, D should be smaller than a predetermined threshold; otherwise we say that a delay fault is detected. Note that the same circuit can detect a delay fault affecting the propagation of a 1/0 transition, the only difference being that the roles of *FIRST* and *LAST* are reversed.

Since the first *OSC* pulse may be generated (possibly as a partial pulse) even when the transitions of *FIRST* and *LAST* are very close, a count of one should *not* be interpreted as indicating a delay fault.

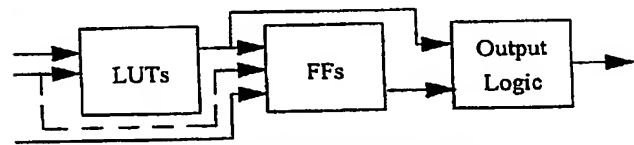


Figure 3. Typical PLB structure

Figure 3 illustrates the typical structure of a PLB, consisting of look-up tables (LUTs), flip-flops (FFs) that can also be configured as latches, and

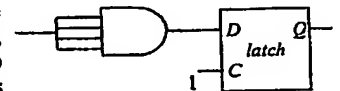


Figure 4. PUT in PLB

output MUX logic. Figure 4 shows the structure of a PUT traversing both a LUT and a FF inside a PLB. The raising input transition is applied to all LUT inputs, and the LUT is configured as an AND gate, whose output propagates the slowest of its input transitions. This allows concurrent testing of all paths through the LUT. The FF/latch is configured as a latch, and its clock input is kept at the active value, so that the latch will be open and will behave like a buffer. In this way the entire PLB implements an identity function. The paths bypassing the FFs and the paths bypassing the LUTs are tested by similar configurations. When propagating a falling transition, the LUT should implement an OR gate.

It is surprising to observe that, unlike ASIC delay-fault testing, our technique does not involve clocking. This is not a problem, since delays on the clock distribution paths are implicitly checked during speed-binning tests. Thus our

delay-fault BIST should be done in addition to, and not as a replacement of, speed-binning.

The BIST circuitry is very simple: the TPG only needs to generate the two transitions, and the *output response analyzer* (ORA) consists of the three gates that produce the oscillation and the counter. The counter is reset before each experiment. Both the TPG and the counter are controlled, and the counter is read, via the FPGA boundary-scan access mechanism.

3. Implementation Issues

The smallest difference between the delay of the fastest and slowest PUTs detectable with our scheme corresponds to one *OSC* cycle. When testing a path with ASIC-type delay-fault testing, the smallest detectable delay fault is generally about 5% of the path delay. To achieve a similar feature, PUTs should be constructed so that their delay corresponds to at least 20 *OSC* cycles.

While making PUTs as long as possible would increase the number of FPGA resources concurrently tested, thus possibly reducing the number of configurations required for a complete test, it may also cause false negative results. For example, assume a path *P1* where all of its components (PLBs, CIPs, and wire segments) are just 1% slower than their counterparts on path *P2*. If the PUTs involve a large number of components, the accumulated difference between the delays of *P1* and *P2* may be reported as a delay fault. Therefore PUTs should be constructed so that their delay is not significantly larger than that of an average "normal" path that would be used in circuits implemented in the FPGA.

In any comparison-based BIST, a passing result may be produced when the compared elements are all faulty; in our case, this means that all the compared PUTs are equally slow. Such a situation is unlikely when we compare several (4 to 8) paths. However, a validation test to protect against this case can be easily done by selecting one of the paths that passed the test and comparing it with a new path which was not part of the compared group.

No delay faults will be detected in a slow device where all paths are equally slow. This is the correct result, and such a chip will be identified by speed-binning and may be allowed to work as a lower speed-grade.

Our approach may fail if a PUT has compensating delay faults, that is, detecting a slow path segment is masked by the presence of a fast segment, so that the overall path delay remains about the same as the other PUTs. In general, however, most delay faults slow down the circuit, and such a multiple fault is unlikely to occur in practice.

The use of the local oscillator created from the inverting feedback in the PLB logic could give rise to concerns of the quality of the clock to the Counter of the ORA. Specifically, the duty cycle and period needed for proper operation of the Counter logic. One solution to this problem is to configure a single flip-flop as a toggle flip-flop with the output of the local oscillator driving the clock input to this flip-flop. This effectively divides the local oscillator frequency by 2 and ensures a near 50% duty cycle. The lower frequency clock will only reduce the resolution of delay fault detection as opposed to preventing this delay fault BIST from working.

However, we have implemented the delay fault BIST approach in an ORCA 2C15A FPGA from Lattice Semiconductor and found the oscillator clock to run at 250MHz while procuring a duty cycle and clock waveform of sufficient quality to obtain reproducible results from one execution of the delay fault BIST sequence to the next. Therefore, dividing the clock may not be necessary.

4. Application to Off-Line and On-Line Testing

Our *roving STARs approach* [1][3] introduced new techniques for on-line FPGA testing, diagnosis, and fault-tolerance, applicable to any FPGA supporting incremental *run-time reconfiguration* (RTR) via its boundary-scan interface [15]. A STAR (self-testing area) is a temporarily off-line section of the FPGA where self-testing occurs without disturbing the normal system activity in the rest of the chip. Roving the STARs periodically brings every section of the FPGA under test. Our approach guarantees complete testing of the FPGA, including all its spare resources, and does not require any part of the chip to be fault-free. In this section, we discuss the application of our delay-fault BIST to roving STARs for delay fault detection.

Figure 5 depicts an FPGA with a vertical STAR (V-STAR) and an horizontal STAR (H-STAR); the system application resides in the working areas denoted by the white boxes representing working PLBs. Note that global horizontal routing resources in V-STAR and global vertical routing resources in H-STAR may be used by the system signals

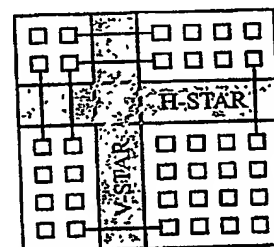
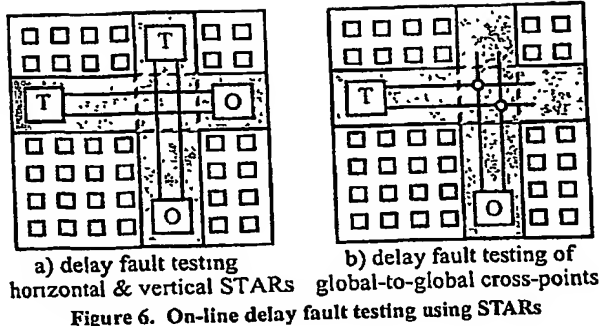


Figure 5. STARs in FPGA

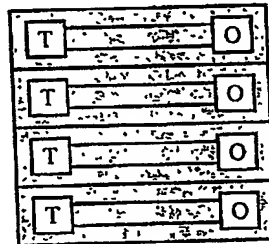
connecting the working areas separated by the STARs. Partial RTR via the boundary scan interface allows the test configurations used by STARs to be downloaded without impacting the system operation. After self-testing of a STAR has been completed (both for PLBs and interconnect), the STAR roves to a new location, by exchanging places with an equal-size slice of the working area; roving the STARs across the FPGA is implemented by a sequence of precomputed partial reconfigurations and assures that the entire FPGA will be eventually tested. The roving process and the use of roving STARs for test and diagnosis of PLBs are described in detail in [1] and [3].

Testing for delay faults follows the pattern of interconnect testing in our on-line routing BIST [11], where horizontal and vertical routing resources are tested in H-STAR and V-STAR, respectively, as illustrated in Figure 6a. Delay faults in the PLBs can also be tested as part of the interconnect delay fault testing sequence. As a result, no additional test phases are required for the PLB logic since these are included when local interconnect delay fault testing is performed. Testing for delay faults in the cross-point CIPs connecting global horizontal and vertical routing busses must involve both STARs and can only be performed at the intersection of the two STARs, as illustrated in Figure 6b. Table 1 summarizes the set of on-line BIST configurations needed for a complete



delay-fault test of a Lattice ORCA 2C series FPGA in terms of the number of test phases that must be executed in each STAR position.

One way of characterizing the difference between on-line and off-line testing is that no system function exists during off-line (manufacturing) testing. Hence for off-line testing, we can populate the entire FPGA with a "galaxy" of parallel STARs (either vertical or horizontal), all executing concurrently the same delay-fault BIST as illustrated in Figure 7.



The entries in Table 1 represent the complete set of delay fault configurations. This set of BIST configurations is the same for both on-line and off-line testing. This is because off-line testing for interconnect is best served by the "galaxy" testing approach and because delay fault testing of the PLB resources (LUTs and latches) can be performed in conjunction with the delay fault testing of local interconnect resources.

Table 1. Summary of delay-fault BIST test sessions

Test Session	Target Faults	No. of VSTAR Phases	No. of HSTAR Phases
1	global routing	7	7
2	local routing & PLB logic	4	4
3	global-to-local interconnections	3	3
4	multiplexer CIPs & PLB logic	7	0
5	cross-point CIPs between global busses		4

5. Conclusions

We have presented the first delay-fault testing approach for FPGAs. The approach is applicable both for off-line manufacturing and system-level testing as well as for on-line testing with our roving STARs approach for fault tolerance. Our approach is based on BIST, it is comprehensive, and does not require expensive ATE. We have successfully implemented this BIST approach on the ORCA 2C series FPGA

and have verified that the approach is not only feasible but also practical. Once delay faults have been detected, the next step for research and development is diagnosis of the delay fault for off-line yield enhancement as well as for fault tolerance for delay faults. this is one of our areas of focus for the future.

References

- [1] M. Abramovici, C. Stroud, S. Wijesuriya, C. Hamilton, and V. Verma, "Using Roving STARs for On-Line Testing and Diagnosis of FPGAs in Fault-Tolerant Applications," *Proc. Int'l. Test Conf.*, pp. 973-982, 1999
- [2] M. Abramovici, C. Stroud, B. Skaggs, and J. Emmert, "Improving On-Line BIST-Based Diagnosis for Roving STARs," *Proc. IEEE Int'l. On-Line Test Workshop*, pp. 31-39, 2000
- [3] M. Abramovici, J. Emmert, and C. Stroud, "Roving STARs: An Integrated Approach to On-Line Testing, Diagnosis, and Fault Tolerance for FPGAs in Adaptive Computing Systems," *Proc. Third NASA/DoD Workshop on Evolvable Hardware*, pp. 73-92, 2001
- [4] M. Abramovici and C. Stroud, "BIST-Based Test and Diagnosis of FPGA Logic Blocks," *IEEE Trans. on VLSI*, Vol. 9, No. 1, pp. 159-172, Feb. 2001.
- [5] J. Emmert, C. Stroud, B. Skaggs, and M. Abramovici, "Dynamic Fault Tolerance in FPGAs via Partial Reconfiguration," *Proc. IEEE Symp. on Field-Programmable Custom Computing Machines*, pp. 165-174, 2000
- [6] J. Emmert, S. Baumgart, P. Kataria, A. Taylor, C. Stroud, M. Abramovici, "On-line Fault Tolerance for FPGA Interconnect with Roving STARs," *IEEE Int'l. Symp. on Defect and Fault Tolerance in VLSI Systems*, pp. 445-454, 2001
- [7] I. Harris, P. Menon, R. Tessier, "BIST-based Delay-Path Testing in FPGA Architectures," *Proc. IEEE Int'l. Test Conf.*, pp. 7-9, 2001
- [8] A. Krasniewski, "Testing FPGA Delay Faults in the System Environment is very Different from Ordinary Delay Fault Testing," *Proc. IEEE Int'l. On-Line Test Workshop*, pp. 7-9, 2001
- [9] H. Michinishi, T. Yokohira, T. Okamoto, T. Inoue, and H. Fujiwara, "A Test Methodology for Interconnect Structures of LUT-Based FPGAs," *Proc. IEEE Asian Test Symp.*, pp. 68-74, 1996
- [10] C. Stroud, S. Konala, P. Chen, and M. Abramovici, "Built-In Self-Test for Programmable Logic Blocks in FPGAs (Finally, A Free Lunch: BIST Without Overhead!)," *Proc. IEEE VLSI Test Symp.*, pp. 387-392, 1996
- [11] C. Stroud, M. Lashinsky, J. Nall, J. Emmert, and M. Abramovici, "On-Line BIST and Diagnosis of FPGA Interconnect Using Roving STARs," *Proc. IEEE Int'l. On-Line Test Workshop*, pp. 31-39, 2001
- [12] C. Stroud, S. Wijesuriya, C. Hamilton, and M. Abramovici, "Built-In Self-Test of FPGA Interconnect," *Proc. Int'l. Test Conf.*, pp. 404-411, 1998
- [13] I. Harris and R. Tessier, "Interconnect Testing in Cluster-Based FPGA Architectures," *Proc. AMC/IEEE Design Automation Conf.*, pp. 49-54, 2000
- [14] I. Harris and R. Tessier, "Diagnosis of Interconnect Faults in Cluster-Based FPGA Architectures," *Proc. IEEE Int'l. Conf. on Computer Aided Design*, pp. 472-476, 2000.
- [15] "Standard Test Access Port and Boundary-Scan Architecture," *IEEE Standard P1149.1*, 1990
- [16] Lattice Semiconductor Co., <http://www.latticesemi.com/products/fpga>
- [17] Xilinx, Inc., <http://www.xilinx.com/products>

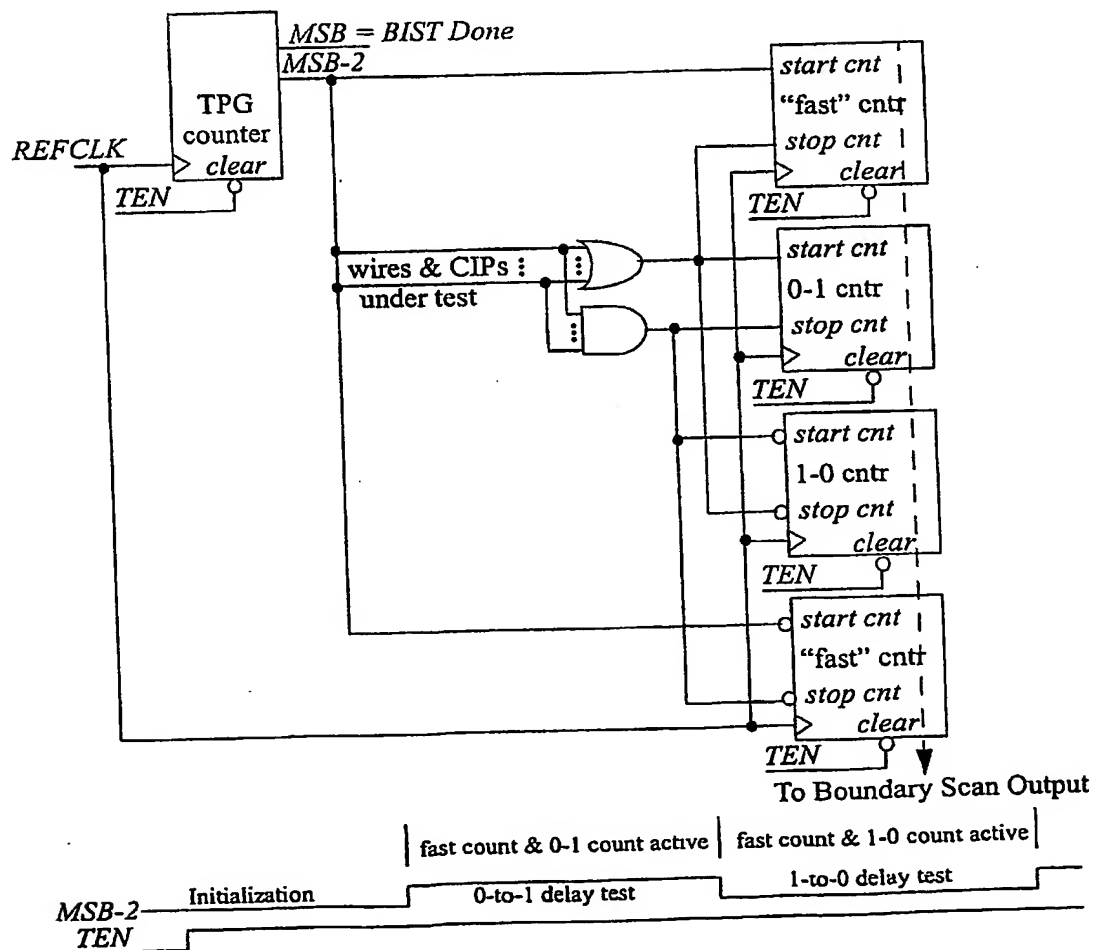
Delay Fault Testing with Both Transitions

Chuck Stroud

The current implementation that Matt did used TEN for the test pattern which allowed the low-to-high transition for the delay fault testing. However, you cannot do the high-to-low transition test since turning off TEN also shuts off the Boundary Scan interface. Therefore to do both transitions you need to have a TPG for the generation of the test signal and the test sequence need to be coordinated with the size of the counters used for the delay fault test (including the comparison of the wires under test as well as the test for a "fast" signal). Therefore, the following test arrangement should work. Given that the maximum expected count values for the "fast" signal test is F and for the regular test is T , then the size of the TPG counter in terms of the number of bits N should be:

$$N \geq \lceil \log_2(F + T) \rceil + 2$$

(EQ 1)



The counter needs to be larger so that the needed control to enable the counts only during the appropriate transition test sequence and then to hold the values in the counters after each transition test sequence is complete. Before taking TEN back low, the count values need to be shifted out of the Boundary Scan interface. Of course this will take some additional logic to control the transfer of the count data from the reference clock (from the on-board oscillator or a high frequency external clock) to TCK. The control logic to the counters and the logic to transfer the data for scanning out on TCK is not shown in the figure.

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